

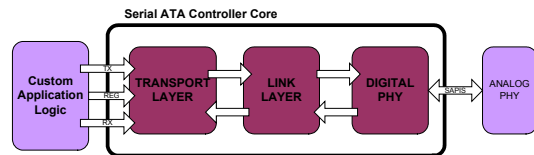
Serial ATA Controller Core

Overview

The Serial ATA (SATA) is a standard storage interface for serially attached storage devices. The Generation I (GEN-I) SATA is defined at speed of 1.5 Gbits/sec and the Generation II (GEN-II) is defined at 3.0 Gbits/sec. StellarIP Solutions Inc. introduces a SATA Controller Core that can be easily integrated to both Host and Device applications. The SATA Controller core described here complies with SATA Specification, Revision 1.0a. The SATA Controller integrates three main components of the SATA functionality namely the Transport layer, Link Layer and Part of the Physical Layer. The Key features of the SATA Controller are listed below.

- Automated Self-checking test environment
- Around 30K ASIC gates for 0.18 TSMC process
- Operates Up to 100MHz Application Clock

Block Diagram



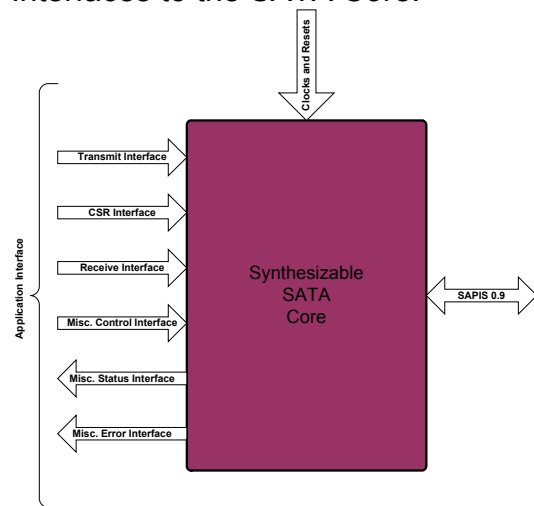
The Analog PHY IP that implements the 2.5Gbps SERDES functionality is available from our partner. The Custom Application logic hosts the DMA Engine and some Serial ATA Host Adapter Specific Registers (SStatus, SError, SControl).

Key Features

- SAPIS Version 0.9 Compliant PHY Interface
- Supports both Host and Device Functionality
- Supports both PIO and DMA modes
- Configurable Transmit and Receive FIFOs
- Elasticity Buffer implemented in Link Layer
- Simple VSIA's PVCi like Slave Interface on the Application Side
- Easily up-gradable to GEN-II SATA
- Implicit timeouts implemented where specification is not clear
- Easy to use DMA interface including DMA hold-off capability
- Implements Shadow Command-Status Block Registers
- Supports both Partial and Slumber Power Management modes
- Mixed Signal PHY available through Partner

Interfaces

Below figure shows the major Interfaces to the SATA Core.



Design Features

- Dual-Scramblers for repeated primitive suppression
- Decodes all the Received FISs, except DMA FISs
- Asynchronous Application Interface
- Verilog based design
- Complete Synchronous Design with no Latches
- Modular Design with clearly defined interfaces
- Consistent coding procedures
- C based Test Environment based on StellarIP's Veriproof™ Technology

Deliverables

- Synthesizable RTL Code for the Core
- Veriproof™ based Test Environment
- Test Vectors
- Ambit Synthesis Scripts
- User Documentation
- Docs On Demand
 - LINT results
 - Code Coverage results

- Test log files
- Complete Test Suite

Support

StellarIP provides only e-mail support. Please e-mail support questions to support@stellarip.com. On-site or phone support is provided on need basis.

For further information on this product, contact StellarIP Solutions Inc. at info@stellarip.com.



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